EAST - [3749a.wsp:1]

File View Edit Tools Window Help

S15: (61) S13 AND (IMPLANTATION IMPLANTING IMPLANTED

Search | List | Browse | Clear

BRS form | IS&R form | Image | Text | HTML

	U	1	Document I	Issue Dat	Page	Title	Current
1	☐	☐	US 2005010	2005051	41	Switching regulator with high-side p-type device	438/305
2	☐	☐	US 2005010	2005051	39	Method of fabricating a lateral double-diffused mosfet (LDMOS) transistor and a conven	438/301
3	☐	☐	US 2005010	2005051	38	Lateral double-diffused MOSFET	438/197
4	☐	☐	US 2005009	2005042	10	High voltage N-LDMOS transistors having shallow trench isolation region	438/197
5	☐	☐	US 2005004	2005022	248	Modular Bipolar-CMOS-DMOS analog integrated circuit and power transistor technolog	438/202
6	☐	☐	US 2005002	2005020	250	Modular bipolar-CMOS-DMOS analog integrated circuit and power transistor technolog	257/328
7	☐	☐	US 2005001	2005012	83	Method of fabricating isolated semiconductor devices in epi-less substrate	438/218
8	☐	☐	US 2005001	2005012	82	Method of fabricating isolated semiconductor devices in epi-less substrate	438/200
9	☐	☐	US 2004026	2004123	8	Semiconductor structure having a compensated resistance in the LDD area and method f	257/368
10	☐	☐	US 2004025	2004122	250	Modular bipolar-CMOS-DMOS analog integrated circuit and power transistor technolog	438/400
11	☐	☐	US 2004025	2004121	251	Modular bipolar-CMOS-DMOS analog integrated circuit and power transistor technolog	257/338
12	☐	☐	US 2004023	2004120	13	Reduced surface field technique for semiconductor devices	257/492
13	☐	☐	US 2004022	2004111	15	ESD protection for semiconductor products	257/365
14	☐	☐	US 2004022	2004111	12	HIGH VOLTAGE N-LDMOS TRANSISTORS HAVING SHALLOW TRENCH ISOLAT	257/510
15	☐	☐	US 2004022	2004111	12	Lateral semiconductor device with low on-resistance and method of making the same	257/333
16	☐	☐	US 2004018	2004091	22	Integrated circuit with a MOS structure having reduced parasitic bipolar transistor action	438/197
17	☐	☐	US 2004011	2004062	40	Semiconductor device and method of manufacturing the same	257/197
18	☐	☐	US 2004010	2004061	13	Integrated circuit structure with improved LDMOS design	257/335
19	☐	☐	US 2004010	2004061	8	High voltage mosfet with laterally varying drain doping and method	257/328
20	☐	☐	US 2004006	2004040	250	Modular bipolar-CMOS-DMOS analog integrated circuit & power transistor technology	438/309
21	☐	☐	US 2004003	2004021	90	Isolated complementary MOS devices in epi-less substrate	438/297
22	☐	☐	US 2004001	2004012	31	Low on-resistance trench lateral MISFET with better switching characteristics and meth	438/193

Hits | Details | HTML

Ready

NUM

EAST - [3749a.wsp:1]

File View Edit Tools Window Help

S15: (61) S13 AND (IMPLANTATION IMPLANTING IMPLANTED

	U	1	Document I	Issue Dat	Page	Title	Current
23	☐	☐	US 2003017	2003091	11	Electrostatic discharge protection in double diffused MOS transistors	438/197
24	☐	☐	US 2003008	2003050	9	Stacked LDD high frequency LDMOSFET	257/565
25	☐	☐	US 2003007	2003041	24	Integrated circuit with a MOS structure having reduced parasitic bipolar transistor action	257/288
26	☐	☐	US 2003000	2003010	11	Electrostatic discharge protection in double diffused MOS transistors	257/330
27	☐	☐	US 2002018	2002121	15	Lateral DMOS structure with lateral extension structure for reduced charge trapping in g	257/409
28	☐	☐	US 2002018	2002121	11	Lateral DMOS structure with lateral extension structure for reduced charge trapping in g	257/402
29	☐	☐	US 2002016	2002110	9	Stacked LDD high frequency LDMOSFET	438/179
30	☐	☐	US 2002013	2002092	9	HIGH VOLTAGE METAL OXIDE DEVICE WITH ENHANCED WELL REGION	438/289
31	☐	☐	US 2002013	2002091	9	Semiconductor device with laterally varying p-top layers	257/341
32	☐	☐	US 2002012	2002091	9	High voltage metal oxide device with multiple p-regions	257/343
33	☐	☐	US 2002011	2002082	31	Low on-resistance trench lateral MISFET with better switching characteristics and meth	257/330
34	☐	☐	US 2002009	2002072	15	High voltage laterally diffused metal oxide semiconductor with improved on resistance a	438/200
35	☐	☐	US 2001003	2001102	10	Radhard power integrated circuit	438/201
36	☐	☐	US 6906381	2005061	13	Lateral semiconductor device with low on-resistance and method of making the same	257/333
37	☐	☐	US 6902967	2005060	21	Integrated circuit with a MOS structure having reduced parasitic bipolar transistor action	438/197
38	☐	☐	US 6900091	2005053	81	Isolated complementary MOS devices in epi-less substrate	438/228
39	☐	☐	US 6894349	2005051	16	Lateral DMOS structure with lateral extension structure for reduced charge trapping in g	257/343
40	☐	☐	US 6876035	2005040	11	High voltage N-LDMOS transistors having shallow trench isolation region	257/343
41	☐	☐	US 6873017	2005032	11	ESD protection for semiconductor products	257/355
42	☐	☐	US 6870218	2005032	13	Integrated circuit structure with improved LDMOS design	257/335
43	☐	☐	US 6855985	2005021	254	Modular bipolar-CMOS-DMOS analog integrated circuit & power transistor technology	257/338
44	☐	☐	US 6835627	2004122	11	Method for forming a DMOS device and a DMOS device	438/302

Ready

EAST - [3749a.wsp:1]

File View Edit Tools Window Help

S15: (61) S13 AND (IMPLANTATION IMPLANTING IMPLANTED I

	U		Document I	Issue Dat	Page	Title	Current
67			US 5701023	1997122	28	Insulated gate semiconductor device typically having subsurface-peaked portion of body	257/341
68			US 5648288	1997071	27	Threshold adjustment in field effect semiconductor devices	438/202
69			US 5648281	1997071	69	Method for forming an isolation structure and a bipolar transistor on a semiconductor su	438/358
70			US 5643820	1997070	67	Method for fabricating an MOS capacitor using zener diode region	438/394
71			US 5618743	1997040	67	MOS transistor having adjusted threshold voltage formed along with other transistors	438/276
72			US 5602046	1997021	20	Integrated zener diode protection structures and fabrication methods for DMOS power d	438/237
73			US 5583061	1996121	67	PMOS transistors with different breakdown voltages formed in the same substrate	438/275
74			US 5559044	1996092	67	BiCDMOS process technology	438/234
75			US 5547880	1996082	68	Method for forming a zener diode region and an isolation region	438/420
76			US 5541125	1996073	68	Method for forming a lateral MOS transistor having lightly doped drain formed along wit	438/202
77			US 5541123	1996073	67	Method for forming a bipolar transistor having selected breakdown voltage	438/202
78			US 5474943	1995121	10	Method for fabricating a short channel trenched DMOS transistor	438/270
79			US 5426328	1995062	60	BICDMOS structures	257/552
80			US 5422508	1995060	57	BiCDMOS structure	257/370
81	☑		US 5416039	1995051	57	Method of making BiCDMOS structures	438/363
82	☑		US 5374569	1994122	65	Method for forming a BiCDMOS	438/203
83	☑		US 5346835	1994091	14	Triple diffused lateral resurf insulated gate field effect transistor compatible with process	438/200
84	☑		US 5341011	1994082	10	Short channel trenched DMOS transistor	257/330
85	☑		US 5300448	1994040	11	High voltage thin film transistor having a linear doping profile and method for making	438/163
86	☑		US 5171705	1992121	5	Self-aligned structure and process for DMOS transistor	438/273
87	☑		US 5134448	1992072	11	MOSFET with substrate source contact	257/330
88	☑		US 5055896	1991100	10	Self-aligned LDD lateral DMOS transistor with high-voltage interconnect capability	257/409

Ready

438/197-203

257

US 1071374907P1

Creation date: 07-06-2005
Indexing Officer: SPOWELL1 - SHUNETTA POWELL
Team: 2800PrintWorkingFolder
Dossier: 10713749

Legal Date: 06-28-2005

No.	Doccode	Number of pages
1	SRNT	2

Total number of pages: 2

Remarks:

Order of re-scan issued on .....